MABB for Network Processors
(Intel® IXP4XX DSP Software Library)

Speaker Name: Xiancheng Yuan
Speaker Title: Product Marketing Manager
Company Name: NPD, Intel Corporation

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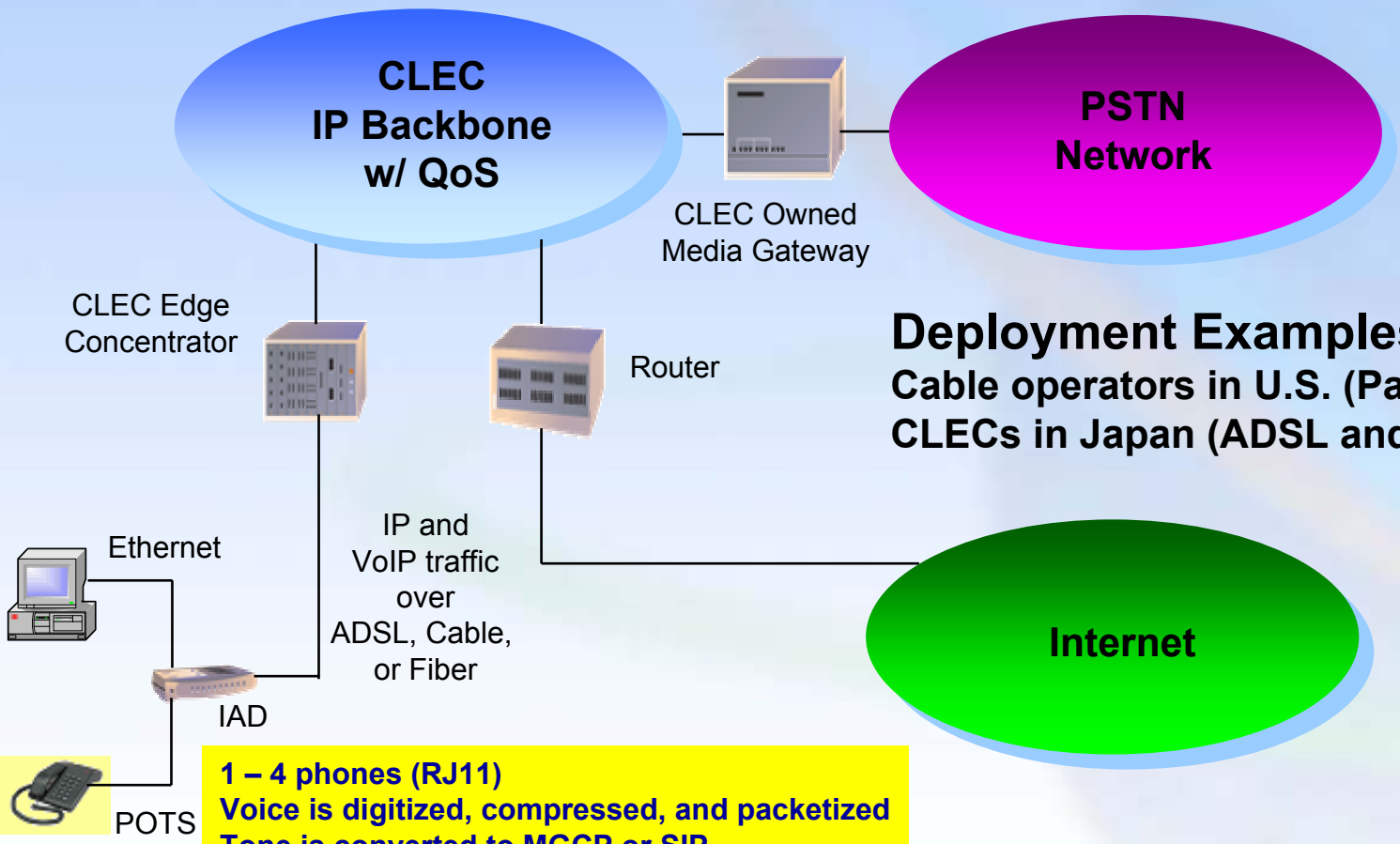
Outline

- Product Vision
- Release 1.0 Features
- Availability and Roadmap
- Demonstration

What is DSR (MABB)

- A component of Intel® IXP4XX Network Processor software library
  - Software based voice and telephony DSP, such as G.729A voice codec, G.168 compliant echo cancellation
- Object library optimized for Intel® XScale™ Microarchitecture
- Two phases:
  - Basic VoIP features with DSR 1.0 release (VxWorks* and Linux* OS support)
  - Enhanced VoIP support with DSR 2.0

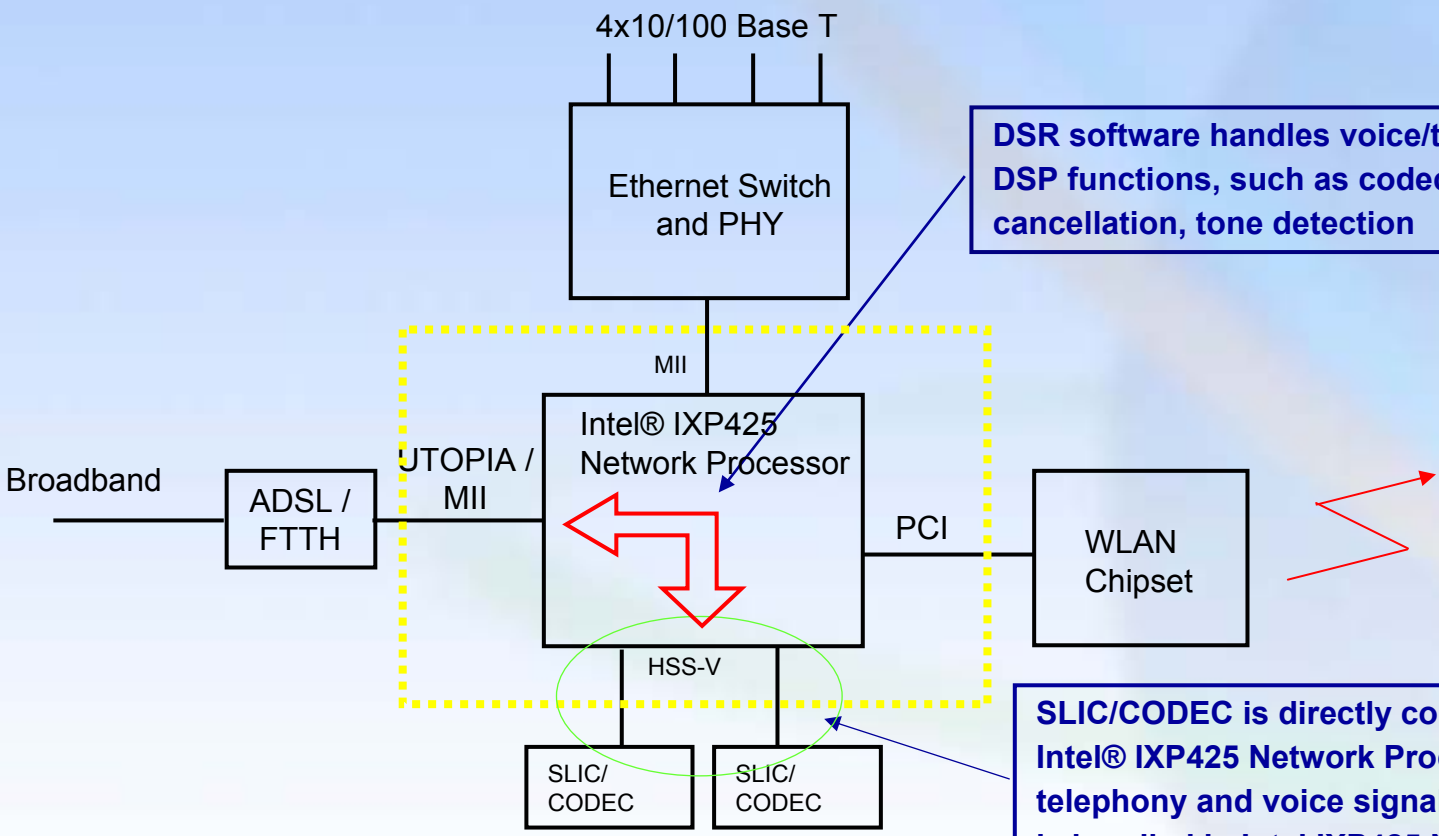
Applications



Deployment Examples:
Cable operators in U.S. (PacketCable)
CLECs in Japan (ADSL and FTTH)

1 – 4 phones (RJ11)
Voice is digitized, compressed, and packetized
Tone is converted to MGCP or SIP
1 – 4 phone lines/numbers
1 – 4 Ethernet (RJ45)
Router/NAT/VPN/Firewallb

An IAD Based on Intel® IXP425

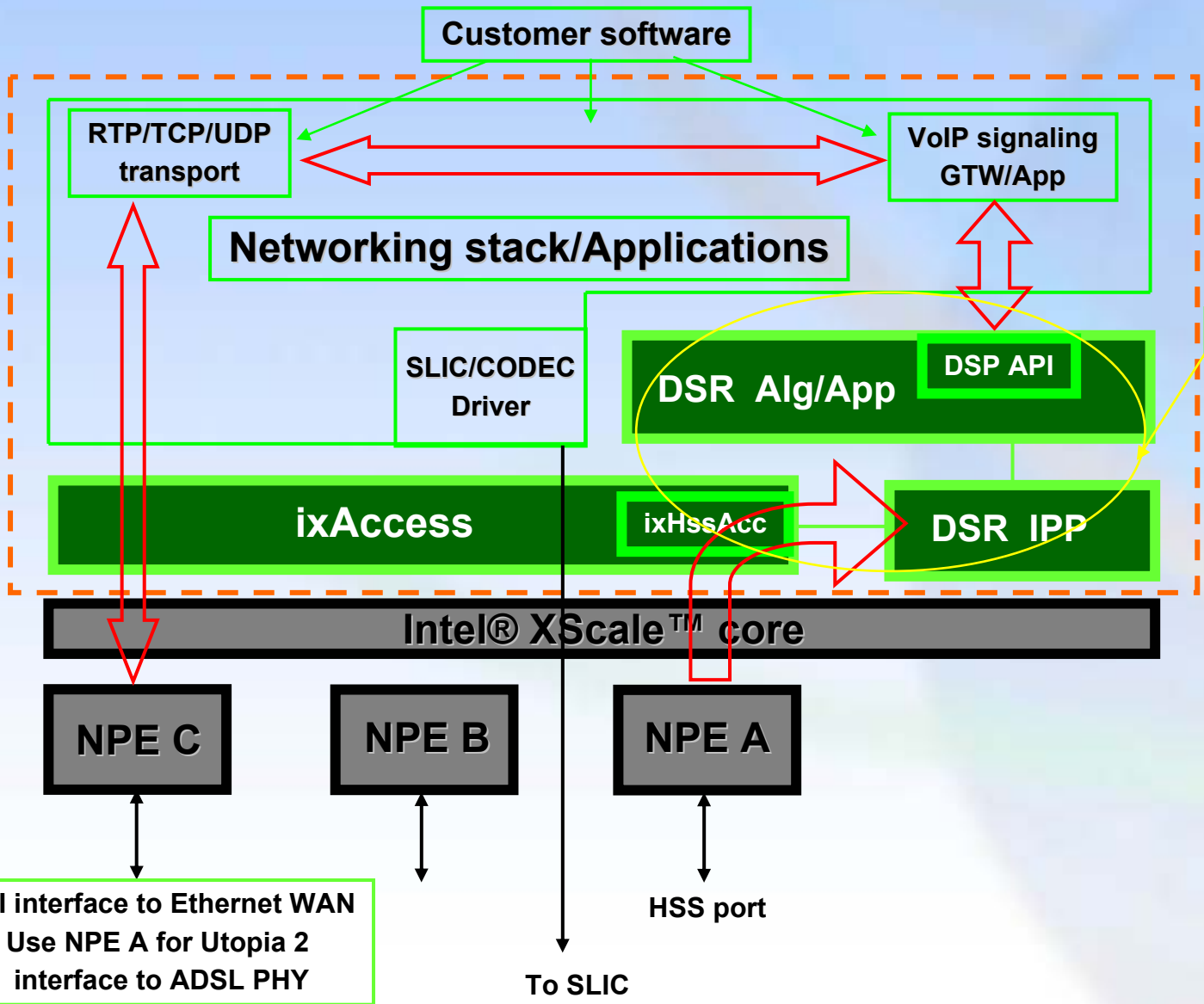


Why DSR (MABB)

- BOM cost savings
  - No need for DSP chip and associated memory
  - DSR 1.0 is software license free
- Seamless integration of secure networking and voice DSP capability improves performance and allows maximum utilization of silicon MIPs
- Simplify development and speed up TTM - one code base instead of separate DSP and networking software
- Other DSR value proposition
  - Highly optimized, field proven Intel IPP technology to provide high performance and interoperability
  - Industry standard DSP API simplifies code porting
  - VxWorks* and Linux* support

DSR (MABB) enables cost effective broadband IAD applications on Intel® IXP421 and Intel® IXP425

DSR 1.0 Software Stack



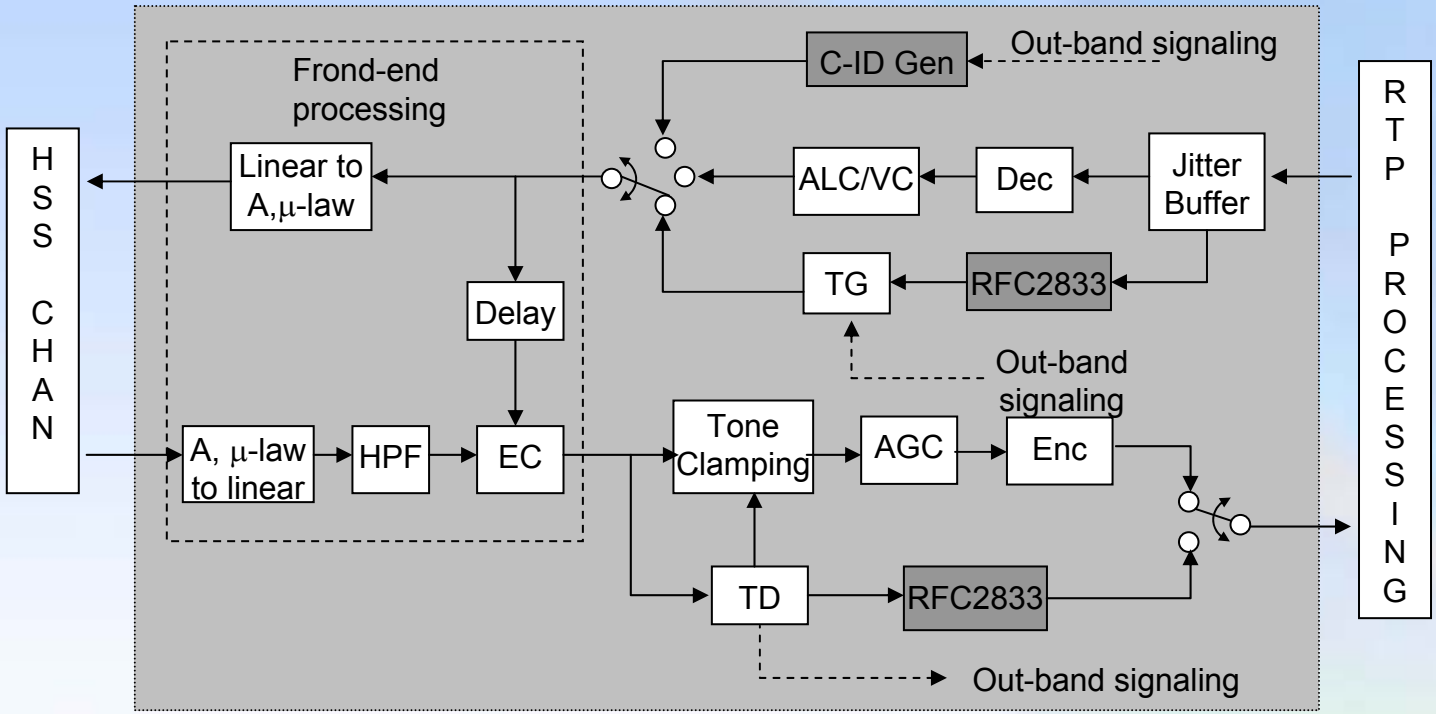
Key DSR 1.0 Features (I)

- Voice Codecs
  - G.711 a/μ law
  - G.729A
- Voice Communication Enhancement
  - Voice Activity Detection (VAD) per G.729B
  - Comfort Noise Generation (CNG) per G.728B
  - Echo Cancellation (EC) per G.168 (8 or 16 ms echo length)
  - Tone Clamping (TC) – Removes DTMF tones from transmitted voice
  - Automatic Level and Gain Control – Regulates transmitted and received voice volume to improve intelligibility

Key DSR 1.0 Features (II)

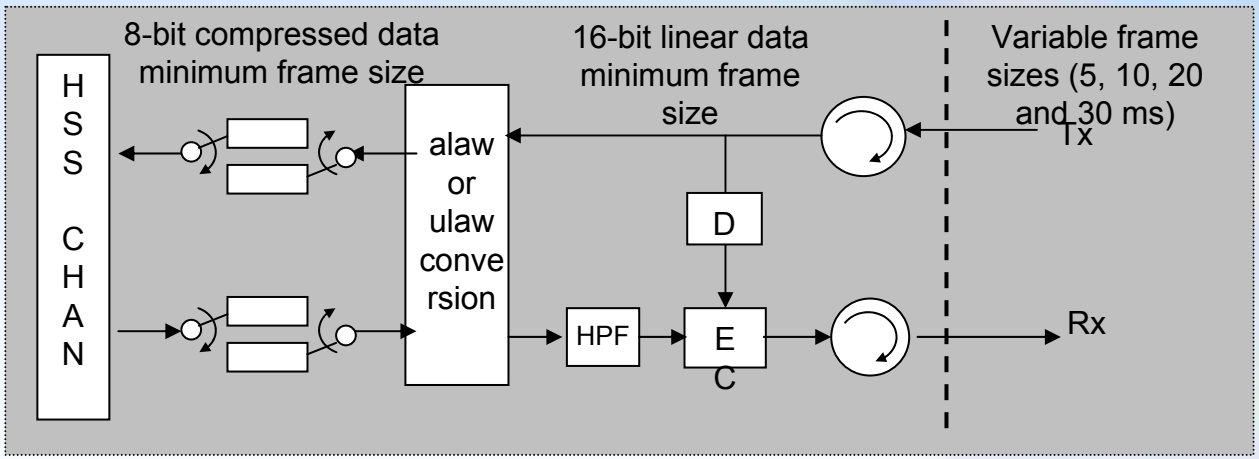
- DTMF Tone Processing
  - Tone generation
  - Tone detection
- Buffering and Framing
  - Dynamic Framing - Supports variable number of voice frames per transmitted voice data packet
  - Dynamic Jitter Buffering – Deals with voice packet transmission jitter and packet loss
- Two voice channels
  - Two simultaneous voice codecs with all necessary associated operations such as VAD, CNG, EC, TC, DTMF, and ALC

Data Flow and Processing



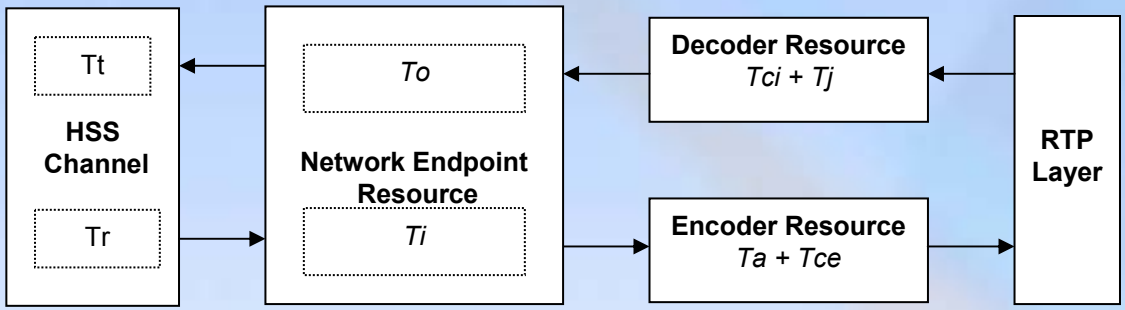
PCM Data Front-End Buffering

- **Performance for Latency, efficiency, and synchronization is maximized using Ping-Pong and Circular buffering techniques**
  - **Ping-Pong buffers are compatible to the HSS device interface**
  - **Circular buffers are used to convert the different data frame sizes between the frond-end process and the other functional blocks**



Understanding Latency

- Latency is a system level issue affecting user-perceived voice quality



- The meanings of each specific delay are described below in detail.
  - *Tt:* *D*elay due to output buffering. It is at 10ms.
  - *To*: Processing and buffering delay of ALC on outgoing data stream. It is at 1ms.
  - *Tci:* Decoding processing delay.
  - *Tj:* Jitter buffering delay, adapt to network conditions, in unit of codec frame (indirectly dependent upon codec): N x frame, where N is an integer.
  - *Tr:* *D*elay due to input frame buffering. It is at 10ms.
  - *Ti*: Processing delay of echo cancellation, etc.
  - *Tce:* Encoding processing delay.
  - *Ta:* Internal codec (look ahead) buffering delay, 5ms for G.729A/B.

DSR 1.0 Performance

Performance Measurement	Requirement	DSR 1.0
MABB MIPS - 2 POTS lines (G.711)	< 50% of 266MHz	15.6%
MABB MIPS - 2 POTS lines (G.729)	< 50% of 266MHz	53% (Beta now at 51%)
Voice Quality - G.711u/EC/TD/ALC/TG/JB (mos/psqm)	>4.4 / <0.3	4.6 / 0.25
Voice Quality - G.711a/EC/TD/ALC/TG/JB (mos/psqm)	>4.4 / <0.3	4.6 / 0.26
Voice Quality - G.729a/EC/TD/ALC/TG/JB (mos/psqm)	>4.0 / <2.2	4.0 / 2.0
End-to-end latency - G.711 call	25ms + JB delay	26.5 + JB delay
End-to-end latency - G.729 call	30ms + JB delay	31.6 + JB delay

MHz indicates IXP425 Xscale core speed

Actual Measurements

VoIP Signaling Protocols

- VoIP signaling NOT covered
  - Example: H.323/H.245/H.225/H.248, MGCP, and SIP
- An area for you to add value

DSR provides comprehensive features and reduces time-to-market

DSR 2.0 Key Features

- Support additional VoIP features
  - RFC 2833
  - Caller ID
  - Call progress tone generation
  - Voice channel mixing

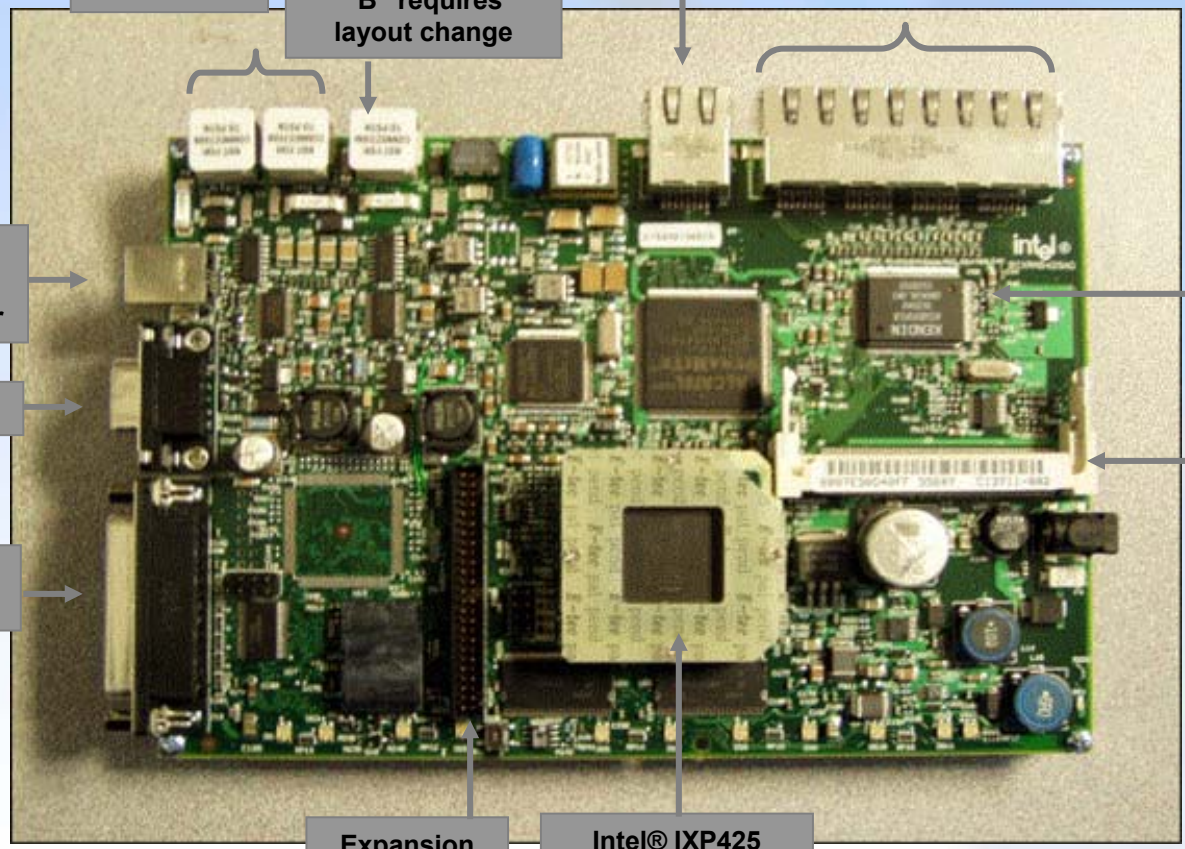
Schedule and Release

- DSR 1.0 release scheduled for late Feb. 2003
  - Early access currently available to Intel® IXP4XX customers and Ecosystem providers
  - Contact your Intel sales representative or NPD BDM, or
  - Contact NPD PME Xiancheng Yuan (xiancheng.yuan@intel.com) or Steve Palermo (stephen.t.palermo@intel.com)
  - Available through FTP download
- DSR 2.0 releases planned for late Q1 or Q2 2003

DSR 1.0 is available now

Demonstration

Gateway Demo Platform with Intel® IXP425

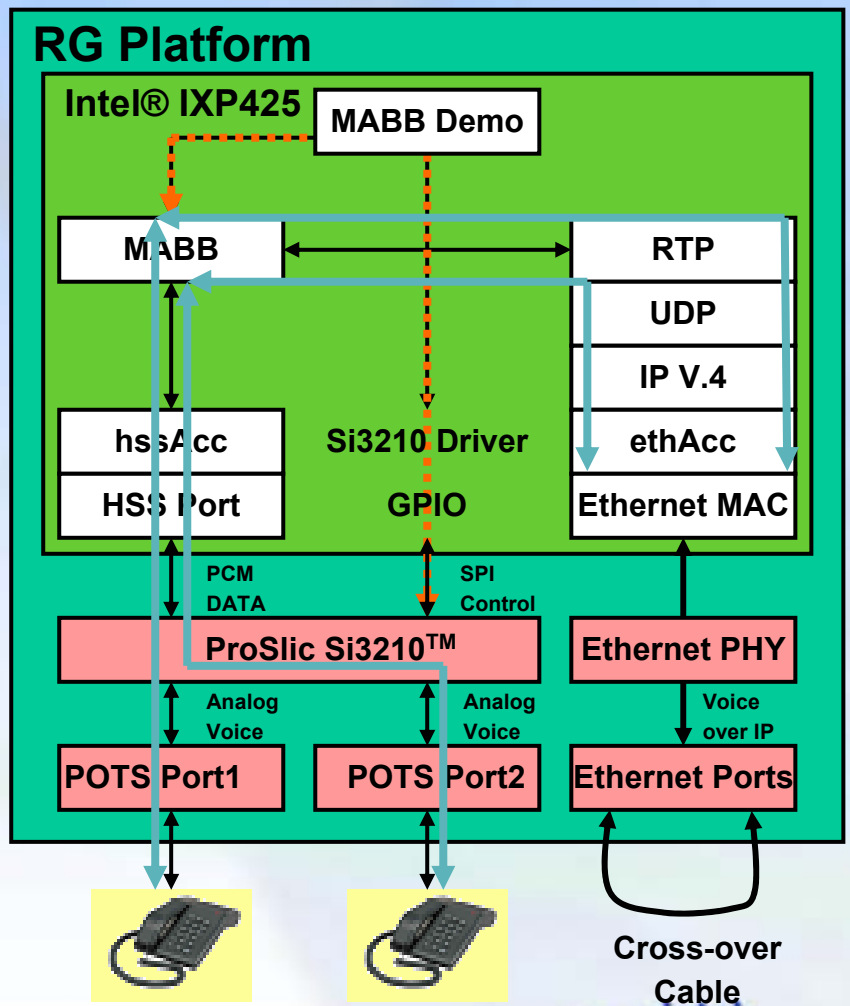


This board will be available from ADI Engineering

Demonstration

DSR 1.0 Loopback Demo

- Demonstrates DSR 1.0 running on the Intel® XScale™ Core with voice in full-duplex
  - A-law or u-law
  - Voice Compression
  - Echo Cancellation
  - Tone Clamping
  - VAD/CNG
  - Simulated end-to-end signaling
- The Demo exercises the VoIP IP Network in a loop-back Mode

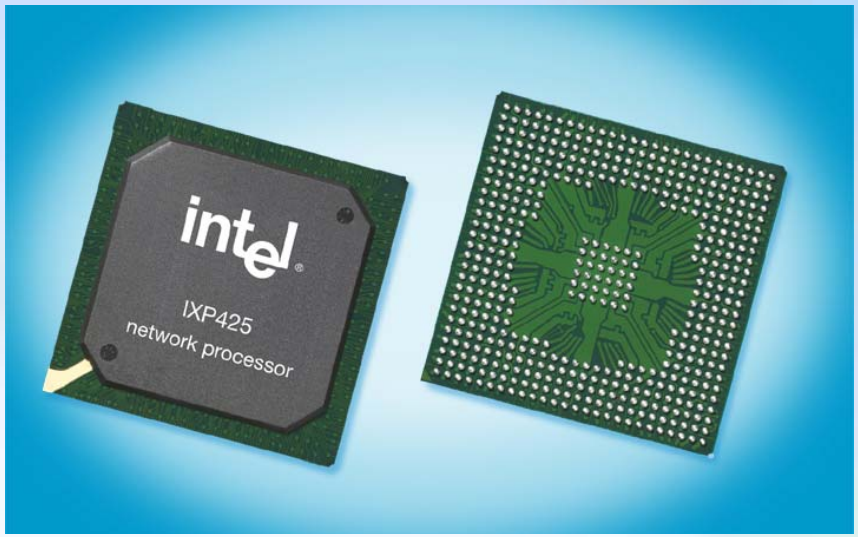


Summary

- DSR expands Intel® IXP4XX network processor solutions to cover voice/telephony DSP for VoIP IAD targeting residential and SOHO market
- The solution enables customers and Ecosystem providers to develop and integrate VoIP capabilities and add their own value features for cost effective and competitive products
- DSR helps customers and Ecosystem providers to improve TTM, cost effectiveness, and product interoperability

- DSR (MABB) enables cost effective broadband IAD applications on Intel® IXP421 and Intel® IXP425
- DSR (MABB) provides comprehensive features and reduces time-to-market
- DSR (MABB) is available now

Visit 5 of the Intel® IXP425-based Demos in Tech Showcase and receive a Free Personal Radio



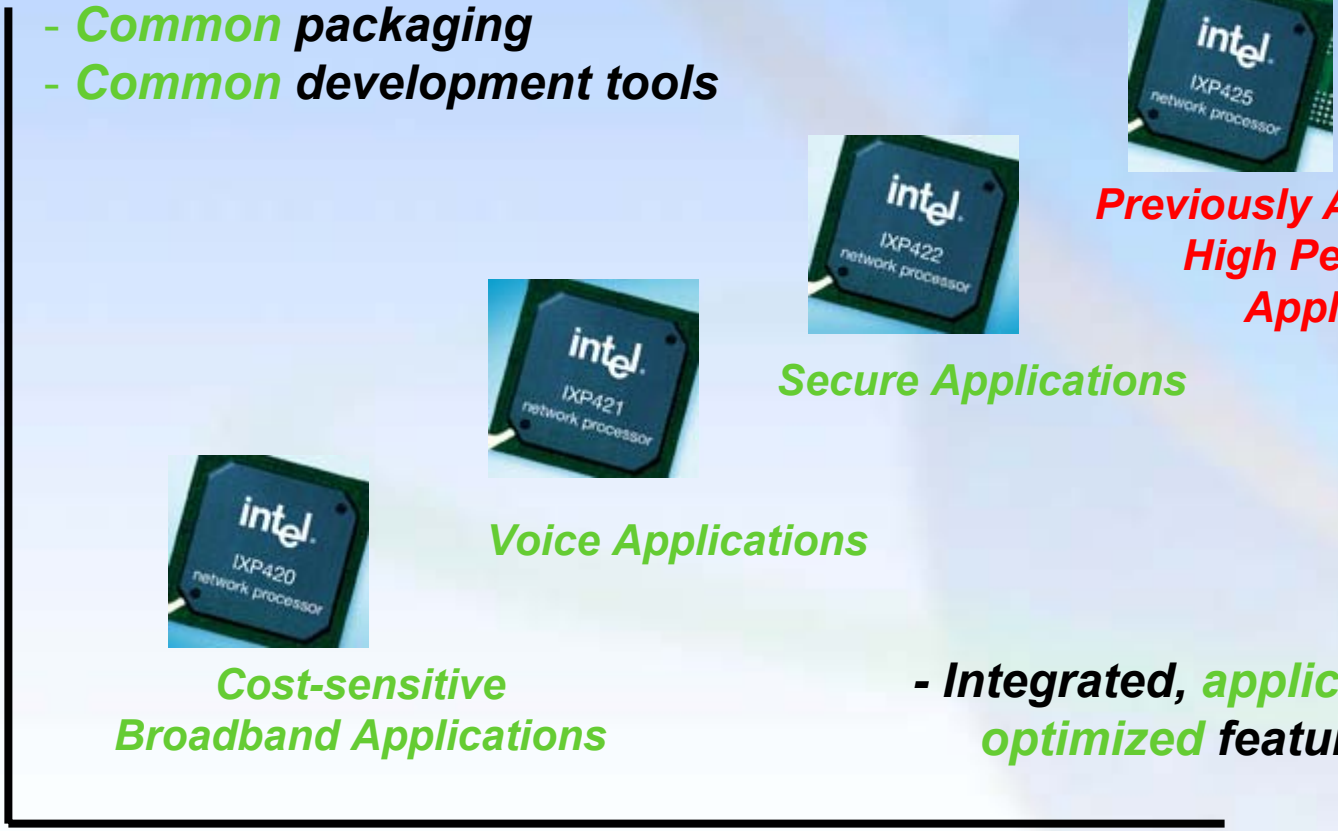
Get a “Game card” in the Intel Pavilion #313 – stand #21 or within the Intel Communications Alliance booth #513

intel

Intel Developer Forum Spring 2003

Intel® IXP4XX Product Line of Network Processors Enables Scalable Performance and Cost

- *Common hardware, software architecture*
- *Common packaging*
- *Common development tools*



Intel® IXP4XX Product Line of Network Processors for Home/SME Applications

- *Intel® 266MHz XScale core for processing headroom*
- *Integrated I/O for ease of configuration*
- *Pin-for-pin compatibility for scalable features*
- *Single platform for lower development cost*

- *speeds up to 533MHz*
- *commercial, extended temperatures*

- *3DES/DES/AES encryption*
- *SHA-1/MD5 authentication*

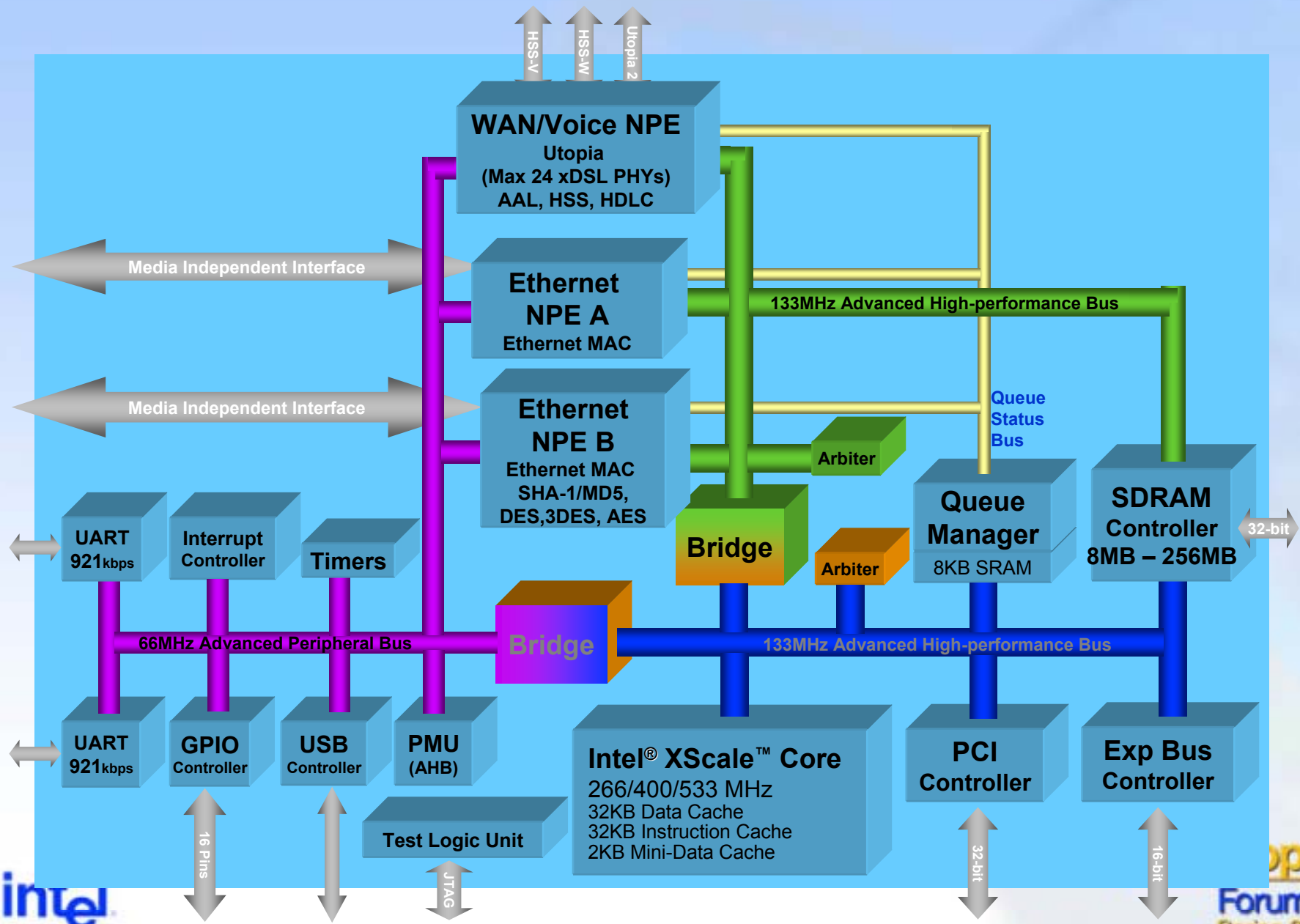
- *up to four VoIP channels*
- *ATM SARing in hardware*
- *two high speed serial ports*

- *two 10/100 Ethernet MACs*

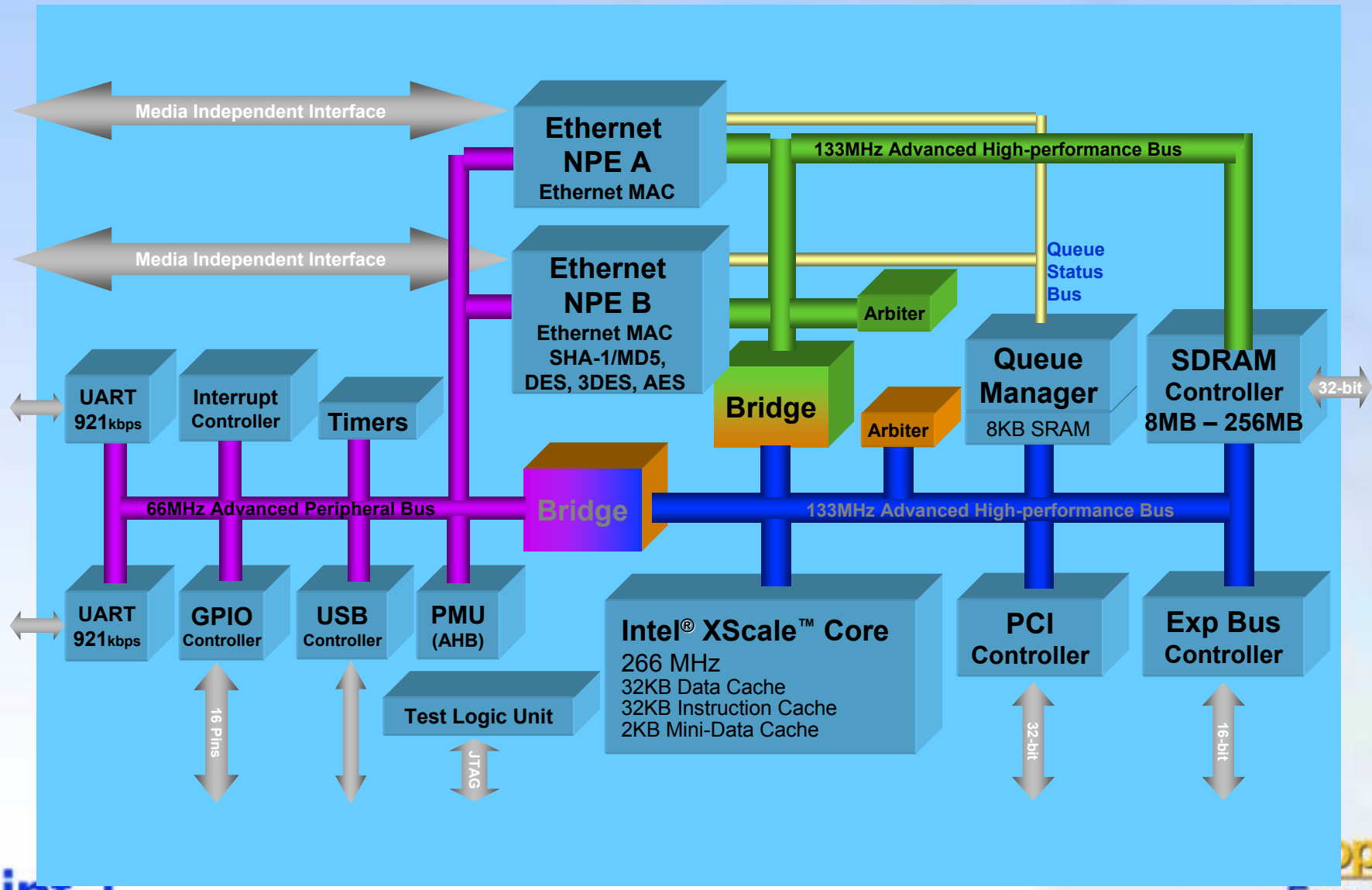
Price

Performance/Features

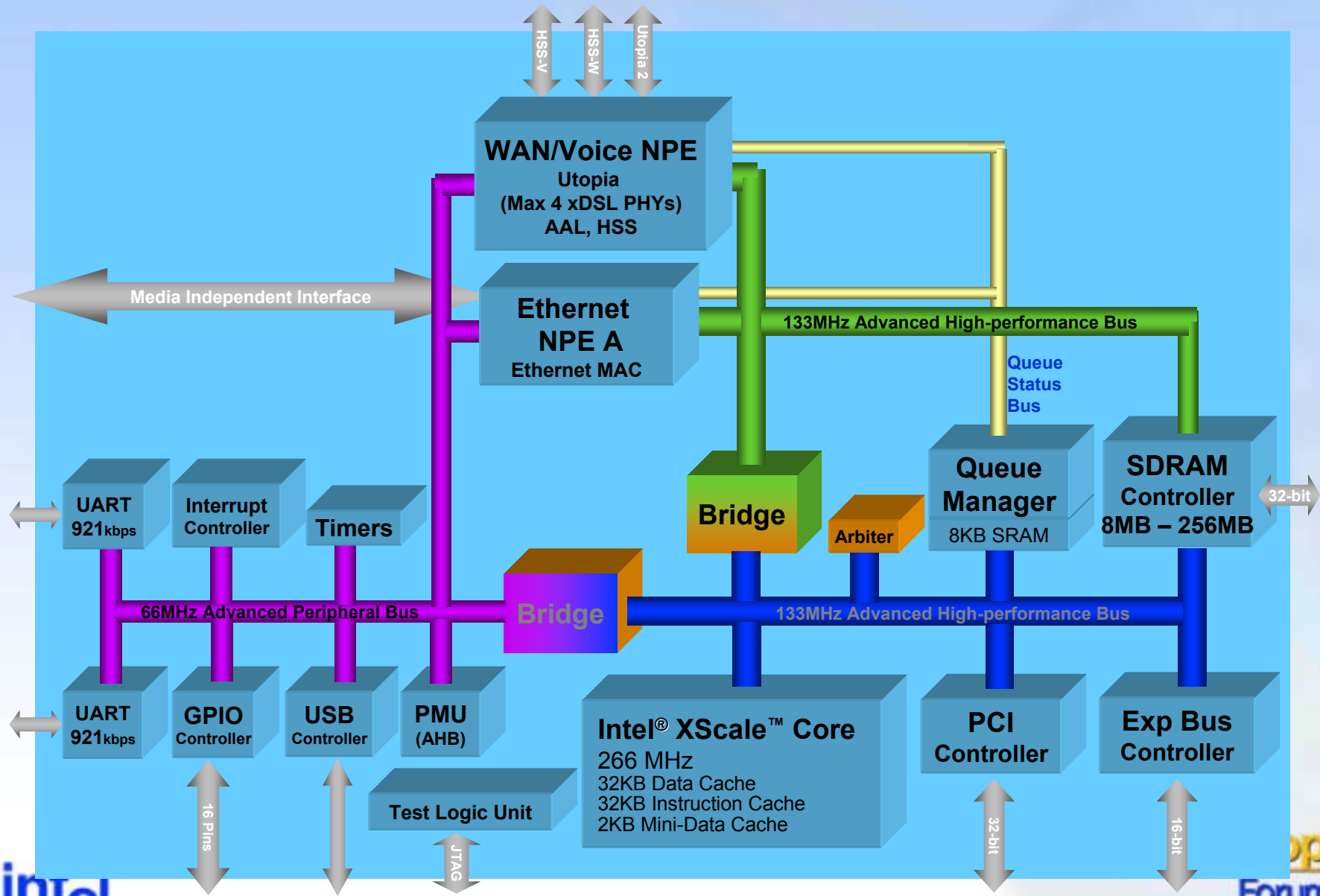
Intel® IXP425 Network Processor Block Diagram (B0 silicon)



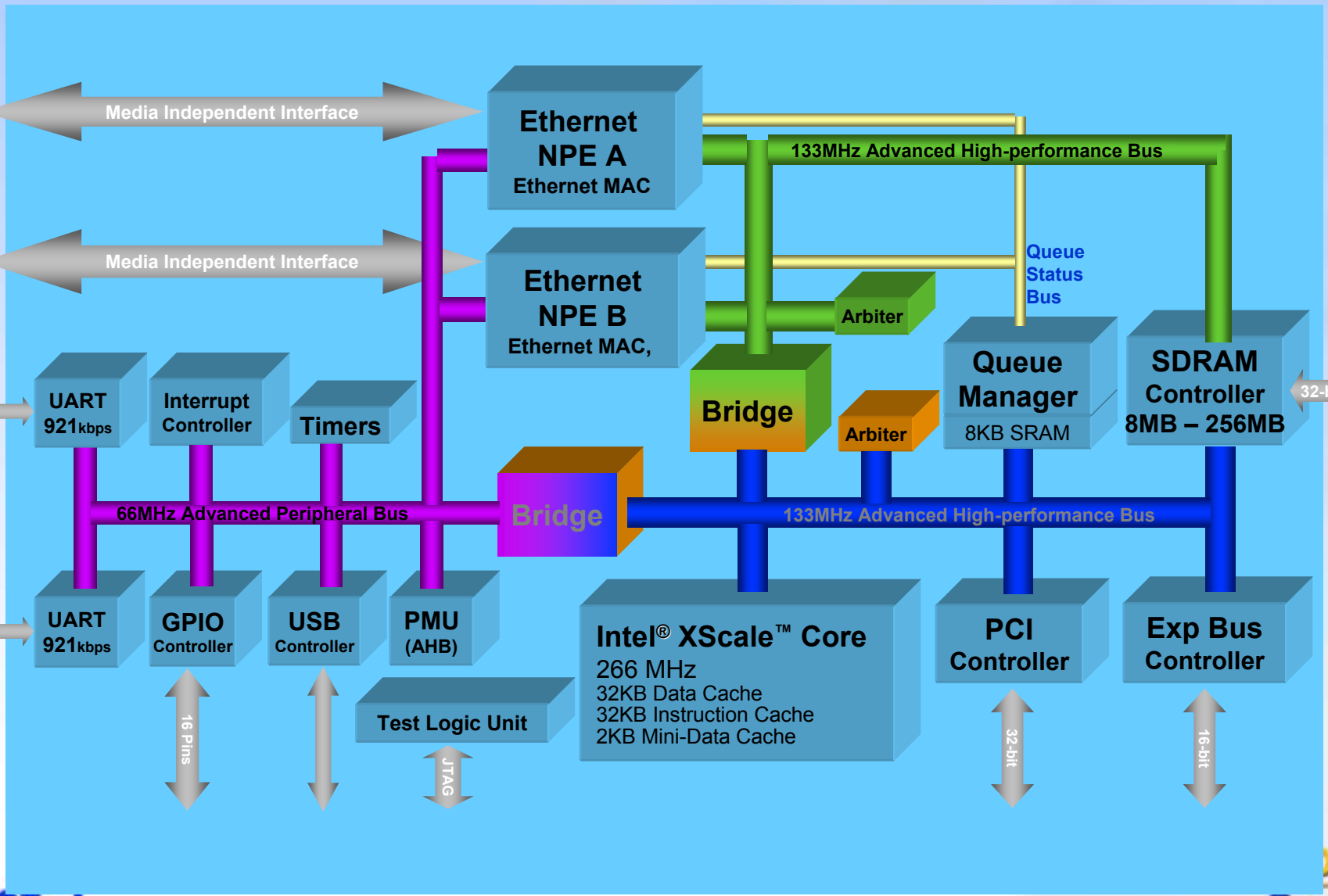
Intel® IXP422 Network Processor Block Diagram



Intel® IXP421 Network Processor Block Diagram



Intel® IXP420 Network Processor Block Diagram



Notice

- Intel has formally named the software product “Intel® IXP4XX DSP Software Library”
- We’ll stop using MABB (Media Application Building Block) naming
- For convenience, sometimes the the acronym DSR (DSP Software Release) is used
- For example: MABB 1.0 release is now DSR 1.0 release

Product Scope

- Intel® IXP4XX DSP Software Library (DSR) is an integral part of Intel® IXP4XX Network Processor software product offering. Its current scope is to provide (software based) voice and telephony DSP capability for the Intel® IXP4XX Network Processors for cost effective VoIP applications
  - Example: G.729A voice codec, G.168 compliant echo cancellation, tone generation/detection
- The software library is optimized to run on the Intel® XScale™ core within the Intel IXP4XX Network Processor. It is released in object code.
- Two implementation phases have been defined so far:
  - Basic VoIP features with DSR 1.0 release (VxWorks* and Linux* OS support)
  - Expanded VoIP support with DSR 2.0 (advanced voice/telephony DSP features)